What is claimed is:

1. A method of making a MOS transistor, the method comprising:

providing a semiconductor substrate comprising a polysilicon gate electrode with a silicide layer thereon, a spacer which is formed on both lateral walls of said polysilicon gate electrode, and source and drain regions with lightly doped drain regions which are formed at both sides of said polysilicon gate electrode;

forming an insulating layer on the area of said substrate including said polysilicon gate electrode;

polishing said insulating layer so that the top of said polysilicon gate electrode is exposed;

etching some part of said insulating layer and said spacer so that both lateral walls of said polysilicon gate electrode are exposed;

forming a metal layer on said substrate resulted from the preceding step so that said polysilicon gate electrode is covered with said metal layer; and

transforming completely said polysilicon gate electrode into a metal silicide gate electrode by performing a thermal treatment process for said substrate coated with said metal layer.

2. A method as defined by claim 1, wherein said spacer and said insulating layer comprise the same material.

3. A method as defined by claim 1, wherein said insulating layer and said spacer are etched until said polysilicon gate electrode is exposed to between about 4/6 and about 5/6 of its height.

4. A method as defined by claim 1, wherein said metal layer comprises a multilayer including transition metals and their alloys.

5. A method as defined by claim 1, wherein said thermal treatment process comprises one or more steps of a rapid thermal process.

6. A method as defined by claim 1, wherein said thermal treatment process is performed at the temperature between about 400℃ and about 600℃ in a first step and between about 800℃ and about 1000℃ in a second step.

7. A MOS transistor comprising:

a gate oxide;

a spacer; and

a gate electrode including a top and lateral walls, wherein the top and some part of lateral walls are exposed.

8. A MOS transistor as defined by claim 7, wherein said gate electrode is fully silicided.

9. A MOS transistor as defined by claim 7 further comprising a metal layer comprising transition metals and their alloys, said metal layer being formed on a surface of said gate electrode.

10. A MOS transistor as defined by claim 9, wherein said gate electrode is fully silicided.

11. A MOS transistor as defined by claim 9, wherein said metal layer has a thickness between about 500 Å and about 1000 Å.

12. A MOS transistor as defined by claim 9, wherein said metal layer comprises one or more of Ti/TiN, Co/TiN and Co/Ti/TiN.

13. A MOS transistor as defined by claim 12, wherein said metal layer has a thickness between about 500 Å and about 1000 Å.